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CS 141: Computing Hardware

Lab 2: ALU

Testing and Simulation methodology

The ALU is tested by iterating over all the possible OP codes and for each OP code passing different values of input X and Y. To begin, the testbench tests the functionality of all the logic gates and the adder by passing the standard case inputs listed below:

1. Two positive numbers: X = 2, Y = 3.
2. A maximum 32-bit number and a zero: X = 4294967295, Y = 0.

The testbench then tests for the following special cases:

1. Two negative numbers: X = -2, Y = -3
2. A positive and a negative number: X = 3, Y= -3
3. A maximum 32-bit number and 1: X = 4294967295, Y = 1

The ALU passed the tests by fulfilling the following expectations:

* The sum of a max 32-bit number and 1 triggered the overflow. The sum of two negative number also triggered the overflow. The same was observed for the sum of a negative and and positive number.
* The logic gates followed the expected outputs as per their respective truth tables.